Design of Miniature Multilayer On-Package Integrated Image-Reject Filters

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***Abstract*—We present the design, implementation, and characterization of compact on-package integrated multilayer image-reject filters. The filter implemented in a novel lumped-element stripline configuration in a standard low-temperature cofired ceramic technology occupies an area of only 3.8 mm × 2.4 mm × 0.5 mm. A distinct feature of this filter is the optimal use of the parasitics of the lumped-element components to implement other components as an integral part of the filter by novel vertical deployments of planar structures. Measurement data of the prototype indicate 3 dB of insertion loss and 20 dB of return loss at the center frequency of 2.4 GHz, as well as 39-dB attenuation at the image frequency, suitable for Bluetooth applications. This paper demonstrates the feasibility of on-package integration of RF front-end elements where the transceiver module is built and, therefore, significantly reduces the development cost.**

***Index Terms*—Bandpass filter, Bluetooth, image-reject filter, low-temperature cofired ceramic (LTCC), lumped-element filter, system-on-package.**

I. Introduction

A SIGNIFICANT portion of the total development cost of a transceiver module is expended on the RF front-end filter typically implemented by discrete components. Integrating filter on-package is an attractive option, especially with the availability of multilevel dielectric systems such as that offered by the low-temperature cofired ceramic (LTCC) process. There are two obvious potential advantages. First, miniaturization is possible by vertical deployment of filter elements since there are several dielectric layers available. Second, it essentially eliminates the need for a discrete filter and, therefore, reduces the component and assembly cost, as well as the assembly time. Furthermore, on-package integrated elements improve reliability due to the reduced probability of solder joint failures.

An on-package-integrated filter, which means a filter integrated on the package substrate housing the transceiver module, offers a better alternative to discrete [1]–[5] and on-chip active filtering with the tradeoff in terms of size, loss performance, power consumption, and dynamic range. An on-chip integrated passive filter [6] occupies large expensive semiconductor real estate, which not only increases the total real estate, but also is not very advantageous in terms of its loss performance considering two factors; first, the low resistivity or the semi-insulating nature of most semiconductor materials and, secondly, the lack of flexibility in allowing large linewidths unlike that given by the multilayer board technologies. An active filter [7], typically implemented on-chip as well, provides gain, but on the other hand, adds the dc power consumption and has a limited dynamic range.

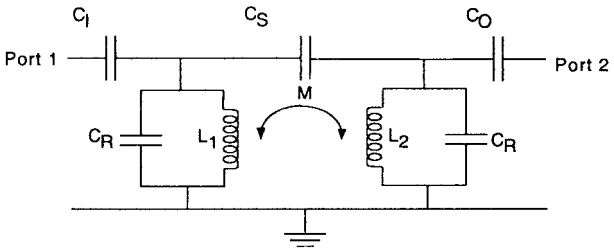

Fig. 1. Schematic of a lumped-element image-reject filter.

The planar filter topology described in this paper offers two distinct features. In addition to it being implemented in a stripline configuration to allow a minimized radiation, it also optimally deploys the lumped components in such a way that their parasitics are used to realize other elements as an integral part of the filter through novel vertical integration. This scheme, described in detail in Section III, allows for a considerable miniaturization compared to, for example, the distributed implementation utilizing cascaded coupled striplines [8], where each segment is a quarter-wavelength long. To the best of our knowledge, this study is the first compact planar S-band LTCC-integrated image-reject filter incorporating the parasitic utilization to implement lumped components. Prototypes have been fabricated and the measurement data discussed in Section IV indicate 3-dB insertion loss and 20-dB return loss at the center frequency of 2.4 GHz, as well as 3-dB attenuation at the image frequency, comparable to commercially available discrete dielectric filters [12] for Bluetooth applications.

II. Circuit Schematic

The lumped-element filter configuration is implemented based on the lumped-element L–C filter circuit. An example of such a topology implementing a top-C-coupled second-order Butterworth configuration is shown in the schematic of an image-reject filter [9] in Fig. 1, which is typically required in a super-heterodyne communication system. In addition to providing transmission within the specified bandwidth, the filter is also required to attenuate the image frequency.

The filter consists of two resonators whose inductors are mutually coupled and three capacitors in the series path. The cre-

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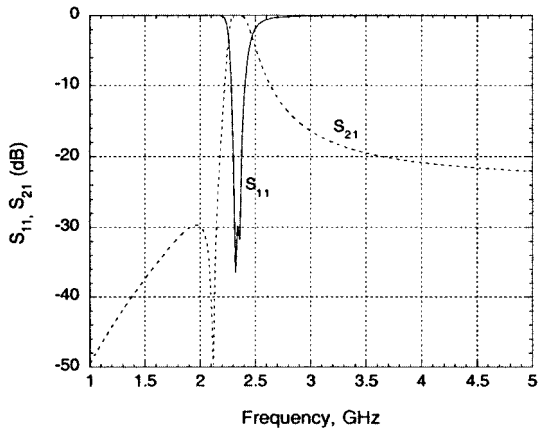

Fig. 2. Filter simulation incorporating ideal elements with $C_I = C_O = 0.6$ pF.

ation of an attenuation pole is realized by using a parallel resonator formed by the combination of magnetic coupling between the resonators and electric coupling by a capacitor [5]. The center frequency and the trap frequency at the image frequency are determined from the transfer function of the filter network. The middle series capacitor C_S is required to set the notch at the desired image frequency given by

$$f_{\text{image}} = \frac{1}{2\pi\sqrt{\dfrac{L_1 L_2 C_S}{M}}} \tag{1}$$

where L_1, L_2, C_S, and M are shown in Fig. 1. The center frequency of the filter is set by the L–C resonators L_1–C_R and L_2–C_R, and the mutual inductance M produced by the coupling between L_1–L_2. The capacitor C_I and C_O are used for impedance matching purposes to set the input and output impedance equal to the external load impedance. The center (f_c) and image (f_{image}) frequencies of the filter was set at 2.45 and 2.175 GHz, respectively, which are the designated carrier and image frequencies of the Bluetooth wireless local area networks (WLANs). The filter parameters L_1, L_2, M, C_R, C_I, C_O, and C_S are 1, 1, and 0.35 nH, and 4.2, 0.6, 0.6, and 1.3 pF, respectively. Fig. 2 plots the response obtained from the simulation of a filter schematic incorporating ideal components.

III. Component Implementation

The next step taken was to implement those components in a multilayer LTCC. The schematic was implemented with six layer of LTCC tapes in a stripline configuration whose three-dimensional view is illustrated in Fig. 3. The tapes are the 3.6-mil-thick Dupont 951ATs with a dielectric constant of 7.8. Two metallization options are available: 6-μm-thick silver and 5-μm wire-bondable gold, of which the silver metallization was chosen for the filter implementation. To help visualize how the filter is deployed, a cross-sectional view along AA' in Fig. 3 is drawn in Fig. 4. Layers 6 and 0 are the top and bottom metallizations, which serve as the top and bottom stripline ground planes. The shunt inductors L_1 and L_2 were realized by the U-shaped strips fabricated on layers 4 and 3, which are two and three layers underneath the top ground plane, respectively.

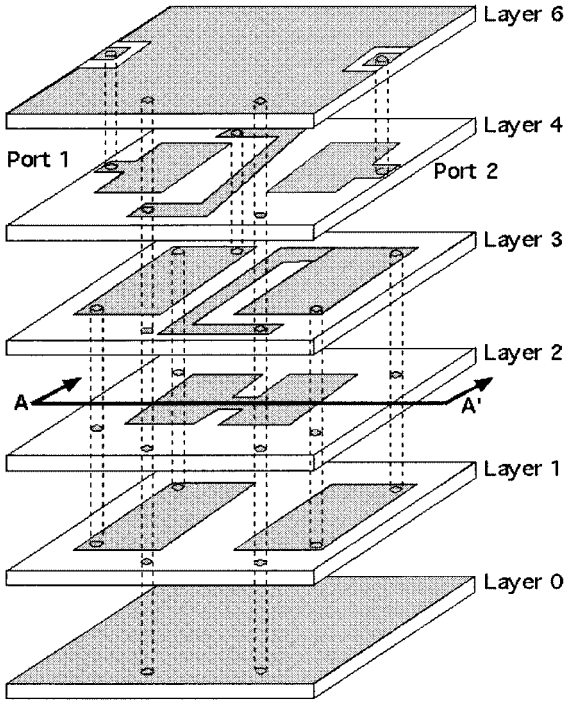

Fig. 3. Three-dimensional layer-by-layer view of a lumped-element multilayer image-reject filter structure.

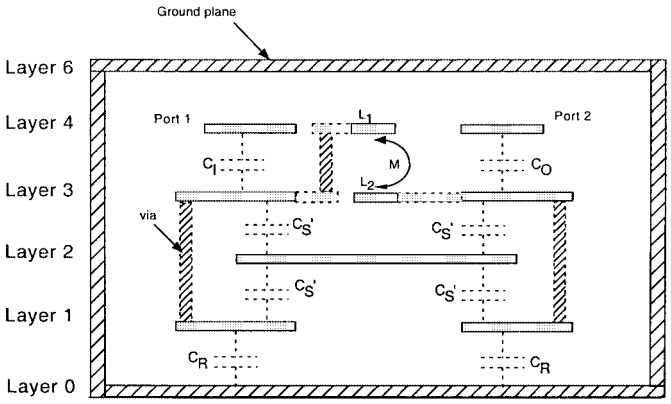

Fig. 4. Cross-sectional view along AA in Fig. 8 indicating how each element in the filter schematic is deployed.

The end of the strips are connected to both grounds through vias. There is no metallization between layers 4 and 6 and, therefore, the top inductor strip on layer 4 is 7.2 mil (two layers) away from the top ground plane, while the bottom strip is 10.8 mil (three layers) away from the bottom ground plane. The required mutual inductive coupling is achieved by overlapping the L_1 and L_2 strips, which is one layer (3.6 mil) apart. Metal–insulator–metal (MIM) capacitors with electrodes on layers 4 and 3 laid out beside the inductor strips were utilized to implement C_I and C_O, as shown in Fig. 3. The rectangular plates on layers 4 and 3 in Fig. 3 serve as the top and bottom plates, respectively, of C_I and C_O. Vertically interdigitated capacitor (VIC) topology was utilized to implement C_S, which is realized by two series capacitors of capacitance $2C_S$. Each of these capacitors is implemented in the VIC topology as a

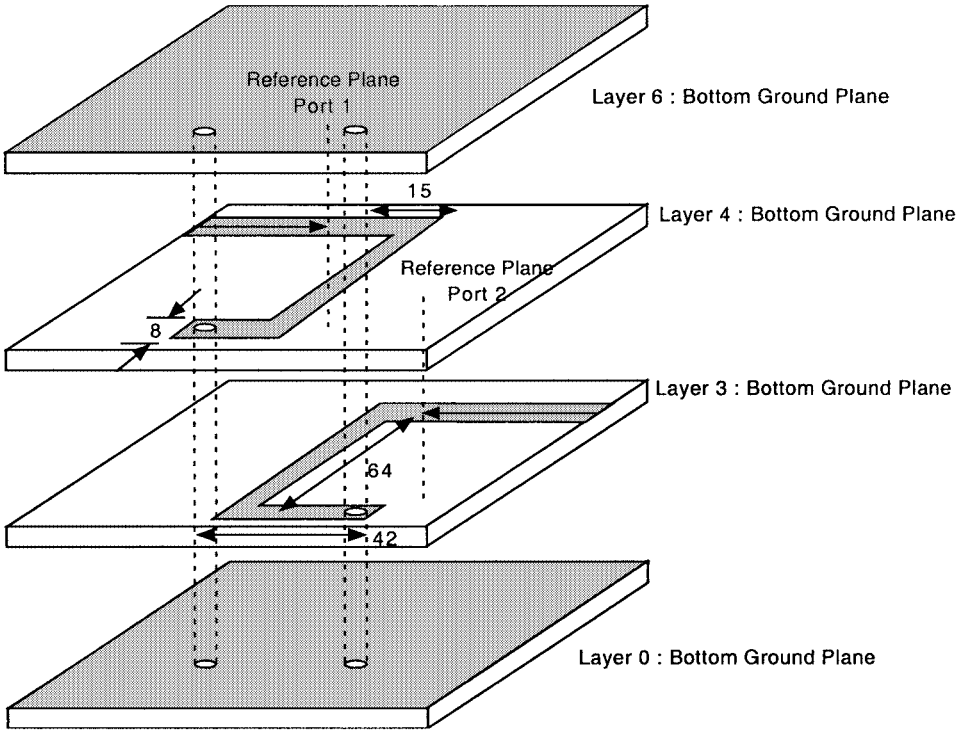

Fig. 5. Inductor topologies implemented to realize L_1 and L_2 and M of the image-reject filter.

parallel combination of two capacitors with a value of C_S. This is depicted more clearly in the cross-sectional view in Fig. 4 showing where the VICs are deployed on layers 3, 2, and 1 underneath C_I and C_O. Such implementation ensures the symmetry of the structure desirable for high-frequency circuits. If C_S were implemented in MIM topology, the entire structure would not have been symmetrical. The bottom plates of C_I and C_O are used as the top plates of the VIC extended to layer 1 through via connections. The "dumb-bell"-shaped trace is inserted on layer 2 between layers 3 and 1 as the bottom plates of the VIC. The plates on layer 3 connected to layer 1 and the plates on layer 3 implementing C'_S are indicated in Fig. 4. The extended top plates of the VIC on layer 1 are used as the top MIM electrodes for the shunt capacitor C_R with the bottom ground on layer 0 as the bottom electrode.

Each component of the filter was built, simulated, and analyzed individually. The drawback of this approach is it does not account for the coupling with the nearby structures. For example, C_I and C_O, when simulated individually, do not take into account the fact that there are additional conductors under them. This individual simulation approach, however, is useful in determining the ideal component values. The first components implemented are the inductors L_1, L_2, and M, whose 3-D view is depicted in Fig. 5 including the dimensions. This structure was drawn and simulated using a commercial method of moments (MoM) simulator [10] with reference planes for input and output ports indicated in Fig. 5. This configuration is not the actual configuration since, in the actual filter topology in Figs. 3 and 4, the coupled inductor strips also see other conductors, which are the bottom plate of the C_S VIC surrounded by other capacitor electrodes.

However, the structure in Fig. 5 itself without taking into account the coupling to other conductors, is useful to estimate the self-inductance and mutual inductance of this configuration. For the first cut design step, the self-inductance is determined by the inductance formula at high frequencies, taking into account the skin effect for a conductor strip sandwiched between two ground planes with equal distance h [11] given by

$$L_{\text{strip}} = \frac{Z_c l}{u} \tag{2}$$

where Z_c is the characteristic impedance of the strip, l is the length of the strip, and u is the wave velocity traveling through the strip given by

$$u = \frac{1}{\sqrt{\mu_o \varepsilon_o \varepsilon_r}} = \frac{c_o}{\sqrt{\varepsilon_r}}. \tag{3}$$

In (3), c_o is the velocity of light in vacuum, μ_o is the vacuum permeability ($4\pi \times 10^{-7}$ H/m), while ε_o and ε_r are the vacuum and relative permitivitty, respectively. The characteristic impedance Z_c in (2) is given as a function of the strip width, conductor thickness, and gap height to the ground plane denoted by w, t, and h, respectively, in (4) [11]

$$Z_c = \frac{\xi}{4\pi} \log \left[1 + \left(\frac{4}{\pi}\right)\left(\frac{b-t}{w'}\right)\left(\frac{8}{\pi}\right)\left(\frac{b-t}{w'}\right) + \sqrt{\left(\frac{8}{\pi}\right)\left(\frac{b-t}{w'}\right) + 6.27} \right]. \tag{4}$$

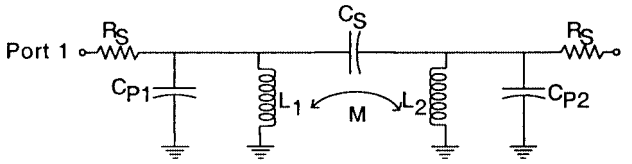

Fig. 6. Circuit model for the overlapping inductor strips implementing the resonator's inductor and mutual inductive coupling.

The parameters in (4) ζ, b, and $(b-t)/w'$ are given by the following equations [11]:

$$\begin{aligned}
\xi &= \sqrt{\frac{\mu_o}{\varepsilon_o \varepsilon_r}} \\
b &= 2h + t \\
\frac{w'}{b-t} &= \frac{w}{b-t} + \frac{\Delta w}{b-t} \\
\frac{\Delta w}{b-t} &= \frac{x}{\pi(1-x)} \\
&\quad \cdot \left\{ 1 + 0.5 \log \left(\frac{x}{2-x} \right)^2 + \left(\frac{0.0796x}{\frac{w}{b} + 1.1x} \right)^m \right\} \\
x &= \frac{t}{b} \\
m &= 2 \left[1 + \left(\frac{2}{3} \right) \left(\frac{x}{1-x} \right) \right]^{-1}.
\end{aligned} \tag{5}$$

In order to realize a 1.0-nH self-inductance, the length of the sheet was calculated from (5) using the parameters w, h, and t in (6) of 8 mil, 7.2 mil (two layers), and 6 μm, respectively. This structure is realized by the "U"-shaped strip shown in Fig. 5 with the total length of approximately 125 mil.

To verify the self-inductance and mutual inductance of the structure shown in Fig. 5, a lumped-element electrical model was extracted after the electromagnetic (EM) simulation was performed. Fig. 6 shows the lumped electrical model for the structure shown in Fig. 5. The model consists of an ideal shunt inductor representing the self-inductance L_1 and L_2 with a mutual inductive coupling of M. R_S represents the conductor loss of the structure, while C_S and C_{P1}–C_{P2} represent the overlapping parasitic capacitance between the two strips and shunt parasitic capacitance to ground, respectively. The required mutual inductive coupling M is given by

$$M = k\sqrt{L_1 L_2} \tag{6}$$

where k in (6) is the coupling factor. If L_1 and L_2 in (6) are assumed to be equal to 1 nH and the desired M is 0.35 nH, then the required k is approximately 0.35, which is realized by optimizing the overlapping strip length between the top and bottom strips. As will be demonstrated later based on the circuit extraction, the overlapping length corresponding to M equals 0.35 nH is 64 mil.

The extracted L_1, L_2, M, R_S, C_{P1}, C_{P2}, and C_S are 1.23, 1.35, and 0.35 nH, 0.2 Ω, and 0.03, 0.05, and 0.2 pF, respectively. There are two reasons why the values for L_1 and L_2 are greater than those predicted by the closed-form equation in (2). First, (2) does not take into account grounding via connecting the strip to both ground planes, which are six layers long or 21.6 mil. Secondly, the h-parameter entered into (5) is 7.2 mil (two layers) since it assumes the strip is located symmetrically between the two ground planes, which is not the case in the real structure.

The capacitors C_I, C_S, and C_R were also simulated individually according to the topology depicted in Fig. 3. Fig. 7 illustrates the three-dimensional view of the three capacitors implemented in the EM simulator. The dimensions indicated in Fig. 7 are for one of four fabricated filters. The dimension of the top plate of C_I and the bottom plate of the VIC implementing C_S were slightly modified in the other three filters to investigate the effects of varying the electrode size. The size of the electrodes was determined using the well-known equation for an ideal square parallel-plate capacitor excluding the fringing effects.

The electrical model of these capacitors is shown in the schematic in Fig. 8. The top schematic is the two-port model for C_I and C_S and the bottom schematic is for C_R. The model consists of an ideal capacitor C_S and parasitic shunt capacitors C_{P1} and C_{P2}. L_S represents the inductance of the capacitor electrode and R_P represents the dielectric loss. Since the electrode width is large, the series resistance representing the conductor loss is assumed to be small enough to be neglected.

The extracted model parameters for C_I are 0.85, 1.1, and 1.2 pF, 0.05 nH, and 1.2 kΩ for C, C_{P1}, C_{P2}, L_S, and R_P, respectively. For C_S, the model parameters are 1.1, 3, and 3 pF, 0.05 nH, and 1.2 kΩ. For C_R, the model parameters are 2.25, 0.2, and 0.02 nH, and 5 kΩ for C, C_{p1}, L_S, and R_P, respectively. Though the shunt parasitic capacitance for the individual capacitor seems to be excessively large and, therefore, the effective capacitance exceeds the desired values, in the actual structures, the parasitic is not as large since the capacitors were shielded by other conductors. For example, the bottom side C_I and C_O are shielded by C_S and, indeed, part of the parasitic capacitance of C_I and C_O were utilized to realize C_S. Likewise, the shunt parasitic capacitance of the VIC implementing C_S is used to implement a shunt C_R. In the previous section, the overlapping sheets used to realize L_1, L_2, and M exhibit a parasitic coupling between the sheets. The parasitic coupling also helps in realizing C_S because it is in the series path of the circuit and, therefore, is in parallel with C_S.

IV. Experimental Data

Fig. 9 shows the photograph of the actual filters with coplanar waveguide (CPW) footprints for on-wafer measurement using air coplanar probes and the top stripline ground plane. Four filters were fabricated; all have the same dimensions for the L_1 and L_2 strips, as well as the size of the electrode for C_R, but have different electrode sizes for C_S and C_I. Table I summarizes the differences among the four filters including the measured performance in terms of the center frequency f_c, insertion and return losses at f_c, image frequency f_{image}, and the corresponding attenuation.

The overall dimension is 5.2 mm $\times$ 3 mm $\times$ 0.5 mm with the CPW measurement pads and 3.8 mm $\times$ 2.4 mm $\times$ 0.5 mm without the measurement pads for all filters. From the summary

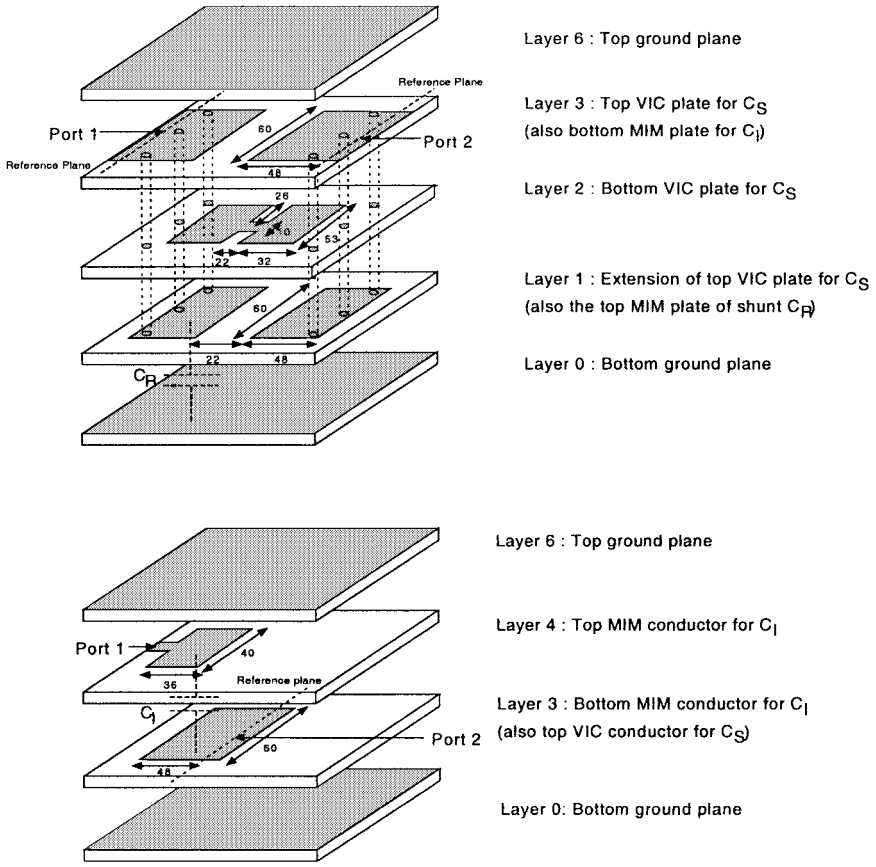

Fig. 7. Three-dimensional views of the stripline capacitors C_S, C_R (top), and C_I (bottom) implemented in MIM and VIC configurations.

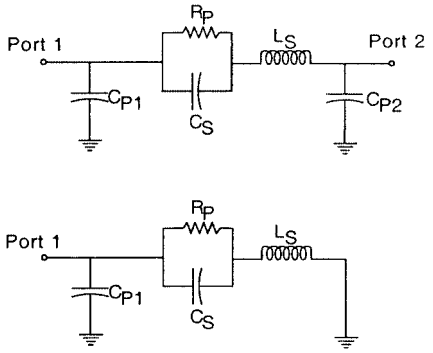

Fig. 8. One- and two-port electrical models of stripline capacitors.

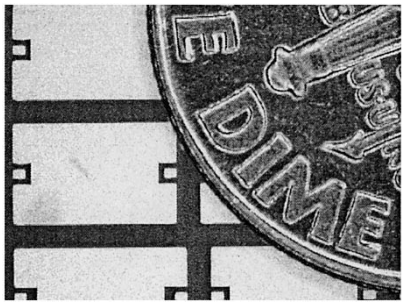

Fig. 9. Photograph of multilayer LTCC Bluetooth image-reject filter prototypes.

outlined in Table I and Figs. 10–13, which show the S-parameters plots of the measured and simulated filters, it is obvious that the center frequency f_c is nearly independent of C_I, C_O, and C_S by noting the small variation for f_c of 40 MHz among the four filters ranging from 2.38 to 2.42 GHz. Slight measured frequency drift both at f_c and f_{image} is observed for all cases attributed to the shrinkage of the conductor trace. This is especially true for the shrinkage of the width of the inductor strip, which yields a slightly larger inductance and, therefore, causes slightly lower f_c and f_{image}. Compared to the specification obtained from a system-level study, filter D is the one that meets all the specifications that require the filter to have a maximum of 3-dB insertion loss, a minimum of 15-dB return loss, and a minimum attenuation of 15 dB at 2.175 GHz, which is the designated image frequency. The measured and simulated filter S-parameters also closely correlate to those simulated using ideal components given in Fig. 2. The insertion loss of 3 dB exhibited by filter D includes the loss introduced by the transition from stripline connecting C_I and C_O to the CPW measurement pads whose parasitic inductance and capacitance also contribute tothe frequency drift. This can be easily corrected by shortening both inductor strips, which not only increases the resonant frequency of the resonator and, therefore, the center frequency of the filter, but also reduces the loss. Even though the notch frequency of filter D is not exactly at the designated image frequency of 2.175 GHz, the attenuation at this frequency is approximately 15 dB, part of which is caused by the lower center frequency. By shortening the inductor strips and thereby increasing the center frequency, the attenuation at 2.175 GHz is expected to be higher as well. The role of C_S in setting the trap

TABLE I
MEASURED PERFORMANCE SUMMARY OF THE FABRICATED LTCC LUMPED-ELEMENT FILTERS

Name	C_I plate size (mil x mil)	C_S plate size (mil x mil)	f_c (GHz)	$\|S_{11}$(dB)$\|$ at fc	$\|S_{21}$(dB)$\|$ at fc	f_{image} (GHz)	$\|S_{21}$(dB)$\|$ at f_{image}
A	36 x 33	32 x 53	2.4	24	3.3	2	41
B	36 x 33	32 x 48	2.4	18	4	2.1	38
C	36 x 30	32 x 45	2.42	18	4.8	2.14	37
D	36 x 40	32 x 53	2.38	20	3.0	2	39

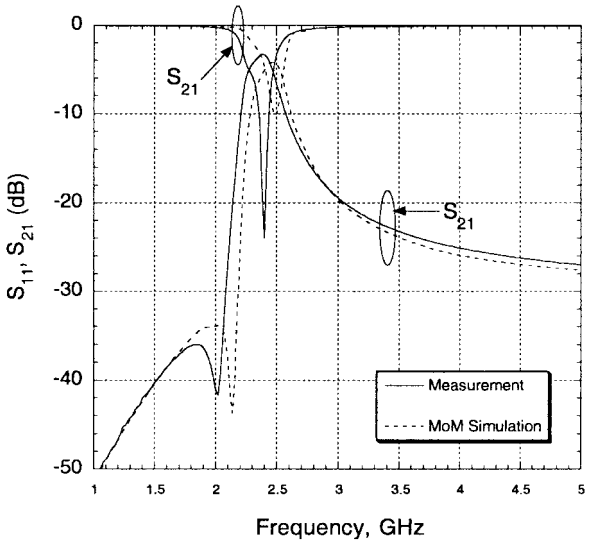

Fig. 10. Measured and simulated magnitude of S_{11} and S_{21} for filter A (C_I plate size: 36 mil × 33 mil, C_S plate size: 32 mil × 53 mil).

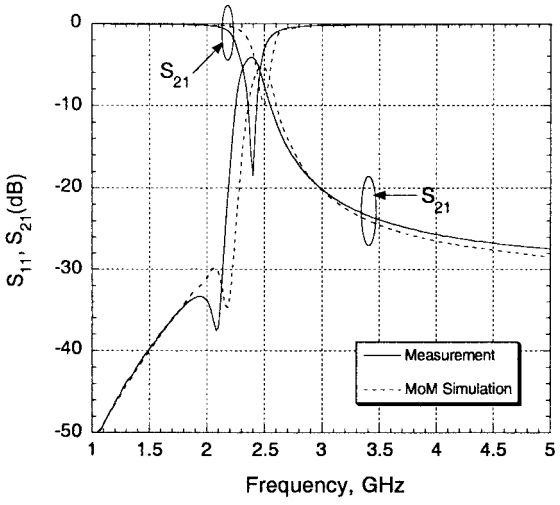

Fig. 11. Measured and simulated magnitude of S_{11} and S_{21} for filter B (C_I plate size: 36 mil × 33 mil, C_S plate size: 32 mil × 48 mil).

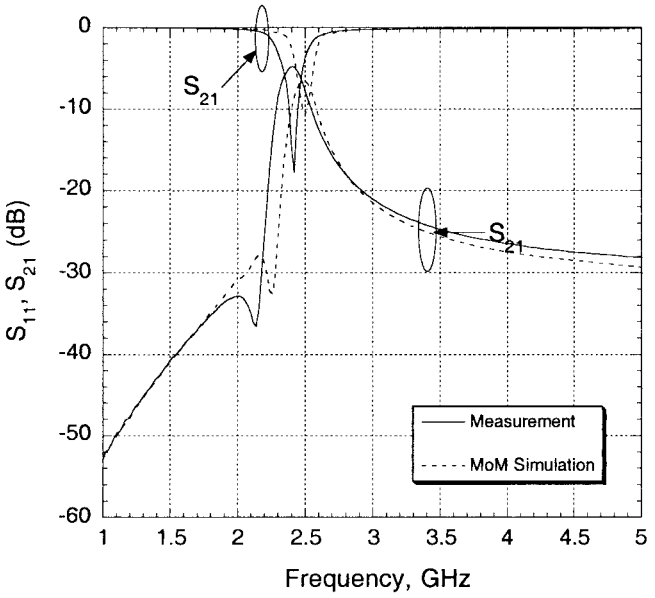

Fig. 12. Measured and simulated magnitude of S_{11} and S_{21} for filter C (C_I plate size: 36 mil × 30 mil, C_S plate size: 32 mil × 45 mil).

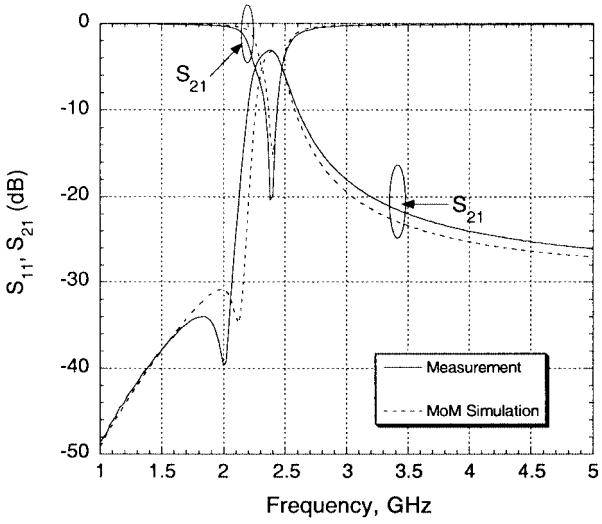

Fig. 13. Measured and simulated magnitude of S_{11} and S_{21} for filter D (C_I plate size: 36 mil × 40 mil, C_S plate size: 32 mil × 53 mil).

frequency can be observed by noting the location of f_{image} and the corresponding size of the bottom electrode of C_S fabricated on layer 2. Filters A and D whose bottom electrode dimension of C_S is 32 mil × 53 mil exhibit f_{image} at 2 GHz with the corresponding attenuation of 41 and 39 dB, respectively. Reducing the electrode dimension to 32 mil × 48 mil and 32 mil × 45 mil increase f_{image} to 2.1 and 2.14 GHz with the corresponding attenuation of 38 and 37 dB for filters B and C, respectively.

It is also noted that increasing f_{image} also increases the insertion loss by looking at 1.5-dB additional loss resulting from reducing the plate size of C_S from 32 mil × 53 mil to 32 mil × 45 mil. This is intuitive since smaller C_S, while yielding higher f_{image} in agreement with (1), provides less transmission or larger impedance at the center frequency. It is also demonstrated that the optimal size of the top electrode of C_I and C_O

on layer 4 that determines their capacitance is 36 mil × 33 mil (Filter A). This configuration yields the best return loss of 24 dB with the tradeoff of 0.3-dB additional loss compared to filter D whose C_I plate has the dimension of 36 mil × 40 mil with the corresponding insertion loss of 3 dB. This is also intuitive considering smaller C_I exhibits higher impedance at f_c and vice versa, which are the case for filters A and D. The insertion loss for filters B and C is exacerbated not only by C_S, but also by C_I, which is beyond the optimum C_I demonstrated by filter A.

V. Conclusions

A compact integrated RF front-end filter implementation on LTCC has been presented. The stripline lumped-element topology allows a higher level of RF module integration, the miniaturization of module size, and the elimination of the need for discrete filters. Several S-band image-reject filter prototypes with a center frequency of 2.4 GHz have been fully characterized and have demonstrated performance suitable for Bluetooth WLAN applications.

Acknowledgment

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